Introduction to Digital Logic

EECS/CSE 31L

**Assignment 1: 1-Bit Decoder**

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**1 Block Description**

This block is deigned to take in an enable and 1 input and decode it into 2 outputs

**2 Input/Output Port Description**

|  |  |  |  |
| --- | --- | --- | --- |
| Port name | Port size | Port Type | Description |
| Enable | 1 | IN | Enable the operation to occur |
| Input0 | 1 | IN | Gets the first operand |
| Output0 | 1 | OUT | The first operation result |
| Output1 | 1 | OUT | The second operation result |

**3 Design Schematics**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Enable | In\_0 | F\_1 | F\_0 |
| 0 | X | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Boolean Expressions:**

F\_0 = (Enable)(In\_0’)

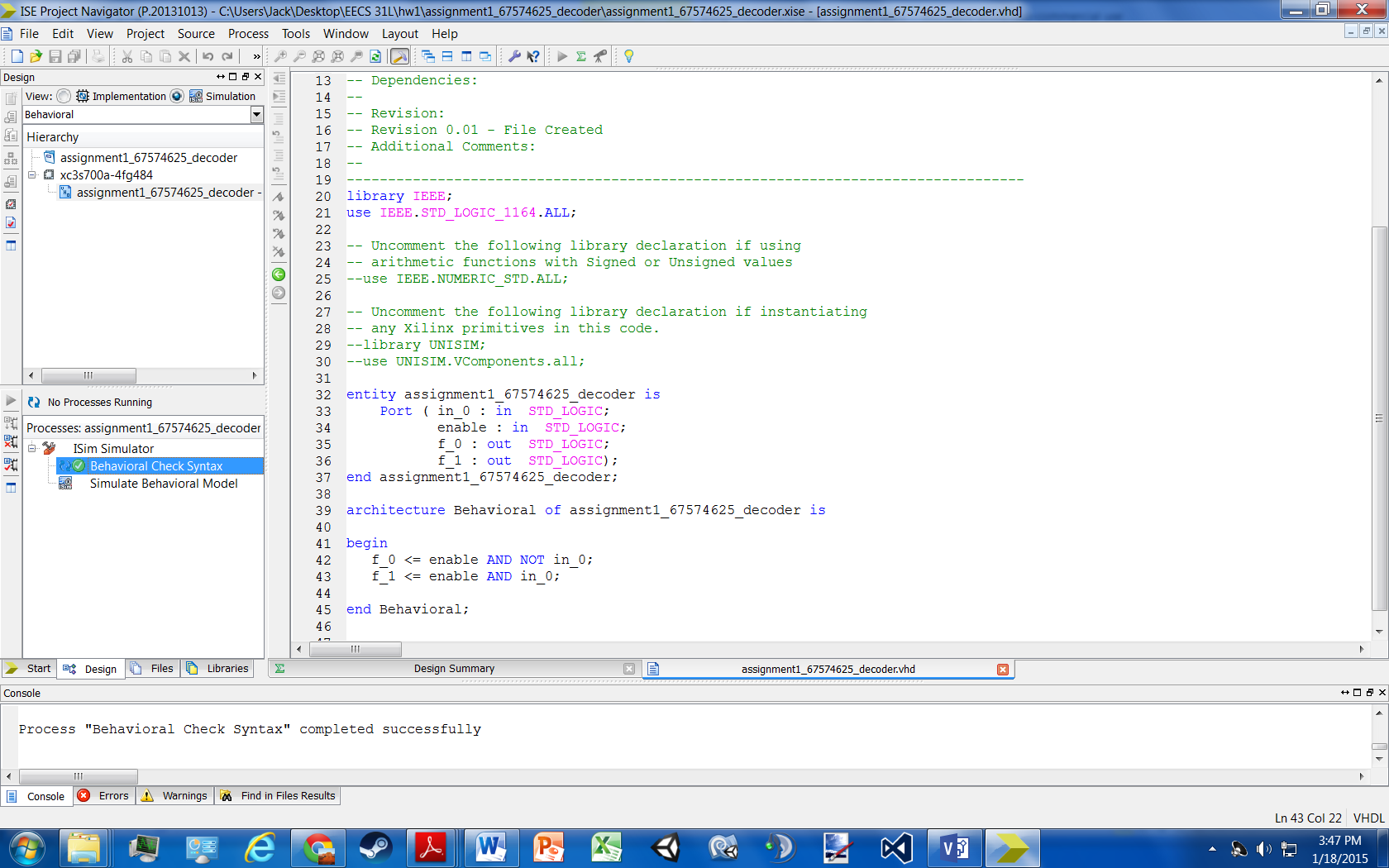
F\_1 = (Enable)(In\_0)

**Gate Representation:**

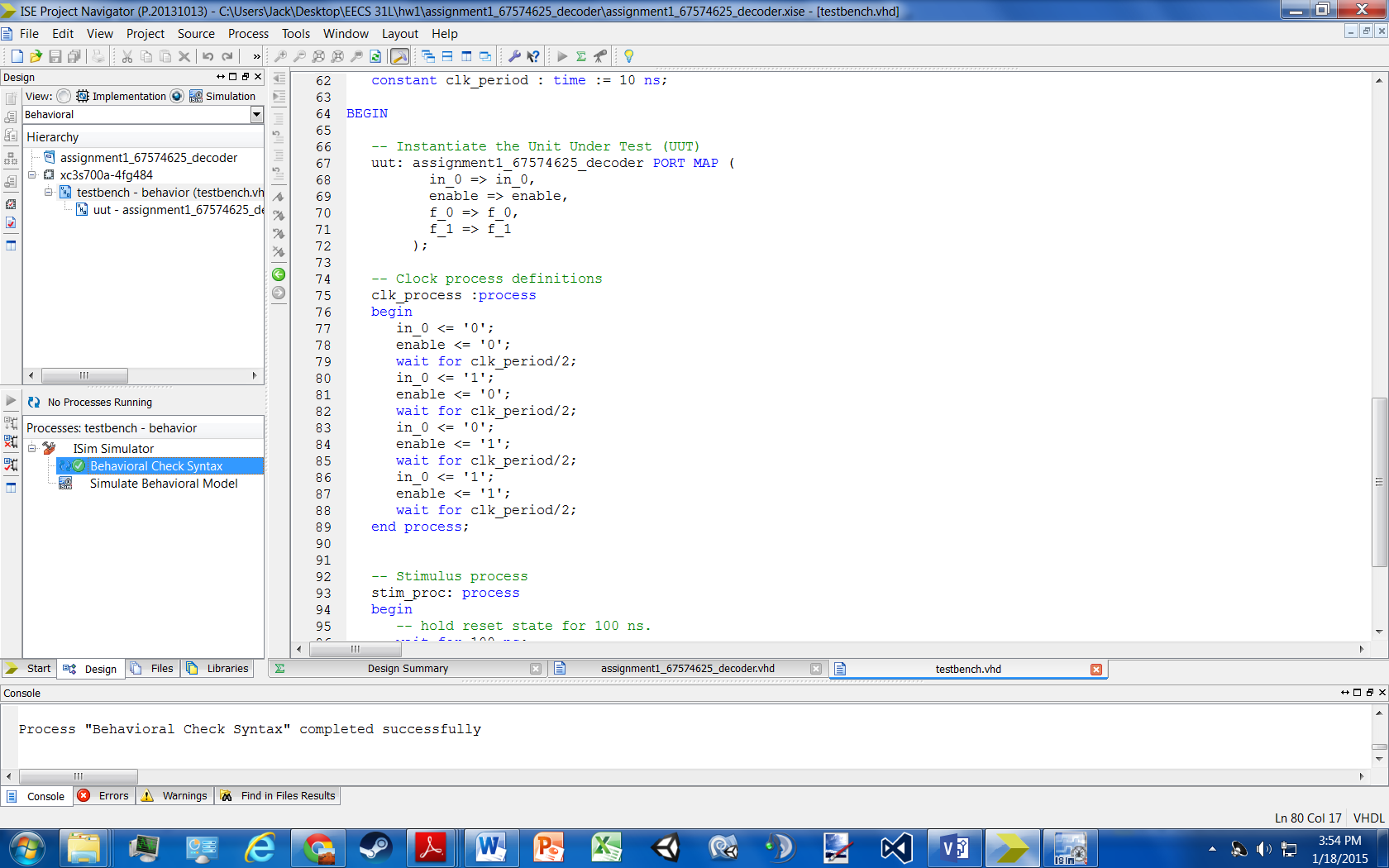


**4 Compilation:**

Decoder compiled



Testbench compiled



**5 Elaboration**

**Assumptions**

* If enable = ‘0’ then both f\_0 = ‘0’ and f\_1 = ‘0’
* If enable = ‘1’ and in\_0 = ‘0’ then f\_0 = ‘1’ and f\_1 = ‘0’
* If enable = ‘1’ and in\_0 = ‘1’ then f\_0 = ‘0’ and f\_1 = ‘1’

**Errors:**

* No errors occurred while coding

**Simulation Log:**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_beh.prj work.testbench

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/assignment1\_67574625\_decoder.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling architecture behavioral of entity assignment1\_67574625\_decoder [assignment1\_67574625\_decoder\_def...]

Compiling architecture behavior of entity testbench

Time Resolution for simulation is 1ps.

Compiled 5 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_isim\_beh.exe

Fuse Memory Usage: 29844 KB

Fuse CPU Usage: 405 ms

Launching ISim simulation engine GUI...

"C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_decoder/testbench\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

**6 Waveform**

